IN THE SPECIFICATION:

Please amend the specification at paragraph [0014] as follows:

[0014] High data rate network 100 supplies high data rate signals to high speed data system 110 and low data rate network 105 supplies low data rate signals to low speed data system 115 each at their respective operating data rate. High-speed data system 110 receives high data rate data signals from the high data rate network 100 and after some processing supplies high data rate signal 120 to node 130. Low-speed data system 115 receives low data rate data signals from the low data rate network 105 and after some processing supplies low data rate ~~signal 120~~ signal 125 to node 130. In one embodiment, high data rate signal 120 and low data rate signal 125 may be digital signals in the form of a square waves encoding data using a pulse or pulse width modulation scheme, however, other wave forms and modulation schemes may be used (e.g. amplitude modulation, phase shift keying, quadrature phase shift keying, and the like).

Please amend the specification at paragraph [0029] as follows:

[0029] In this embodiment, capacitors 550a and 550b are connected to apply the input differential data signals from the transmission lines 500a and 500b to the nodes formed as the common connections of the bases of transistors 532a and 532b, the resistors 565a and 565b, and the resistors 545a and 545b that are each connected in series with capacitors 535a and 535b. Resistors 565a and 565b have a resistance of about 50 K-ohm and resistors 545a and 545b have a resistance of about 50 ohm. Capacitors 550a and 550b have a capacitance of about 5uF and capacitors 535a and 535b have a capacitance of about 100nF and are connected to the reference node of voltage source 560 and to resistors 565a and 565b.

Voltage source 560 supplies the system bias voltage 570 (Vcc). In this embodiment, the combinations of capacitors 535a and 535b with resistors 545a and 545b determine the short time constants for each branch of the differential signals. These time constants control the response of the interface system 520 to the 2.5 Gbps data signals with the associated square wave transitions. Similarly, the long time constants for each branch of the differential signals are determined by the combination of capacitors 550a and 550b with the large-value resistors 565a and 565b. These time constants control the response of ~~interface system 530~~ the interface system 520 to the 9.6 Kbps data signals with longer periods between square wave transitions.